Am79R79 Ringing SLIC User's Guide



Application Note

The Am79R79 Ringing SLIC (RSLIC) provides cost-effective ringing support in short loop applications. It includes circuits for two- to four-wire conversion; loop and ring-trip detection; programmable DC feed and two-wire impedance; battery switching; and relay drivers. The Am79R79 RSLIC can generate a trapezoidal ringing voltage sufficient for 5REN (ringer equivalent number), or $1.4 \text{ k}\Omega$.

For details on features and specifications, consult the Am79R79 Ringing SLIC Data Sheet. For more information on designing with the Am79R79 RSLIC, refer to the application note, Am79R79 Ringing SLIC Technical Overview. These documents assume familiarity with the structure and terminology of the telephone system. For general telephony information, refer to Understanding Telephone Electronics. Additional references are listed at the end of this document.

INTRODUCTION

This note describes the process of external component selection of the Am79R79 RSLIC, including enough theory of operation information to customize your circuit for a particular application.

This note shows you how to calculate the values of the external components, which influence the cost and form factor of the design. Variations might include 3REN versus 5REN, 70 V versus 60 V supply, 100 Ω versus 200 Ω loop length, 40 mA supply versus 120 mA supply, square wave versus trapezoid, etc.

There are three sets of parameters to program the Am79R79 RSLIC: DC, AC, and ringing. DC parameters include loop detect and DC feed characteristics. The AC parameters comprise two-wire input impedance, transhybrid loss, receive path gain, and transmit path gain. Ringing parameters include crest factor, ring-trip detection, and ring current limit. The ringing requirements also dictate the power supply voltage and its current capability.

DC CHARACTERISTICS

Current Limit

The current from the RDC pin into the RSN node controls the current feeding into the loop. Set the DC current limit with resistors R_{DC1} and R_{DC2} . C_{DC} provides DC control loop stability and some filtering. A nominal value for the loop current is 25 mA. Figure 1 shows the DC current feed.

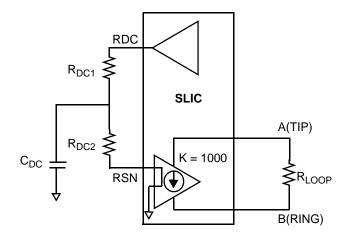


Figure 1. DC Current Feed

The current flowing in the loop is:

$$I_{\text{LOOP}} = \frac{V_{\text{RDC}}}{(R_{\text{DC1}} + R_{\text{DC2}})} \bullet 1000$$

where V_{RDC} is -2.5 V when a loop is established at the nominal operating point, and K = 1000.

Choose C_{DC} such that the time constant τ_{DC} , formed by the parallel combination of R_{DC1} and R_{DC2} with C_{DC} , is 16–30 ms.

$$C_{DC} = \tau_{DC} \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$$

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DC Feed

The Am79R79 RSLIC is a battery-switching SLIC. High battery is used in the Ringing state and to meet on-hook open circuit voltage specifications. While in the Off-Hook state, switch the device to low battery to save power.

Under normal off-hook conditions, the Am79R79 RSLIC operates in the constant-current region. As loop length increases (R_{LOOP}), so does V_{AB} (see Figure 2; notice that $V_{AB} = V_A - V_B$). Above V_{ASL} (for low battery) and V_{ASH} (for high battery), the anti-saturation circuitry reduces the current to prevent saturation and clipping in the amplifiers. This overhead is programmable by connecting the resistors R_{SGH} (for high battery) and R_{SGL} (for low battery) to pins RSGH and RSGL, respectively. If RSGH and RSGL are left open, then $V_{ASL} = 12.5 \text{ V}$, $V_{ASH} = 44 \text{ V}$, $V_{APPL} = 16.7 \text{ V}$, and $V_{APPH} = 48.2 \text{ V}$, which suffices for most applications.

You can raise the anti-saturation portion of the high battery curve by tying R_{SGH} to ground; lower this portion by tying R_{SGH} to $V_{CC}.$ You also raise or lower the anti-saturation region of the low battery curve by tying R_{SGL} to ground or $V_{CC},$ respectively.

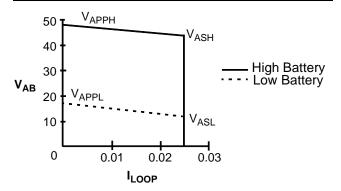


Figure 2. DC Feed

If V_{ASHH} is defined as $V_{ASH} - V_{ASL}$, and with R_{SGH} and R_{SGL} grounded (raising the curve(s)):

$$V_{ASL} = \frac{1000 \cdot (104 \cdot 10^{3} + R_{SGL})}{6.72 \cdot 10^{6} + 80 \cdot R_{SGL}}$$

$$V_{APPL} = V_{ASL} + 4.17$$

$$V_{ASHH} = \frac{1000 \cdot (70 \cdot 10^{3} + R_{SGH})}{1.934 \cdot 10^{6} + 31.75 \cdot R_{SGH}}$$

$$V_{ASH} = V_{ASL} + V_{ASHH}$$

$$V_{APPH} = V_{ASH} + 4.17$$

With R_{SGH}, R_{SGL} tied to V_{CC} (lowering the curve(s)):

$$V_{ASL} = \frac{1000 \cdot (R_{SGL} - 56 \cdot 10^{3})}{6.72 \cdot 10^{6} + 80 \cdot R_{SGL}}$$

$$V_{APPL} = V_{ASL} + 4.17$$

$$V_{ASHH} = \frac{1000 \cdot (2.75 \cdot 10^{3} + R_{SGH})}{1.934 \cdot 10^{6} + 31.75 \cdot R_{SGH}}$$

$$V_{ASH} = V_{ASL} + V_{ASHH}$$

$$V_{APPH} = V_{ASH} + 4.17$$

If R_{SGH} and R_{SGL} are connected to V_{CC}, they must be at least 100 k Ω .

Loop Detect

This function indicates an off-hook condition in all but the Ringing and Open Circuit states. Refer to the *Ringing* section on page 6 for a discussion of ring-trip detect. In the Active, Standby, and OHT (on-hook transmission) states, the resistor $R_{\rm D}$ controls loop detect. For the Active and OHT states, the following equation applies:

$$\frac{\left|I_{LOOP}\right|}{300} \bullet R_D = \frac{V_{AB}}{\alpha}$$

If the active battery is V_{BAT1} , the value of α is 1/12.67, and if the battery is V_{BAT2} , the value of α is 1/11.37. The loop current equals V_{AB} divided by the resistance in the loop, as shown in the equations below. Let R_{LTH} be the desired threshold resistance for loop detect, R_{SL} be the resistance of the wires in the loop, and R_F be the fuse resistors. For most applications, the following values suffice: $R_{LTH} = 5 \, k\Omega$, $R_{SL} = 70 \, \Omega$, and $R_F = 50 \, \Omega$.

$$I_{LOOP} = \frac{V_{AB}}{R_{I,TH} + R_{SI} + 2R_{F}}$$

So, for V_{BAT1},

$$R_D = (R_{ITH} + R_{SI} + 2R_F) \bullet 12.67$$

and for V_{BAT2},

$$R_D = (R_{I,TH} + R_{SI} + 2R_E) \cdot 11.37$$

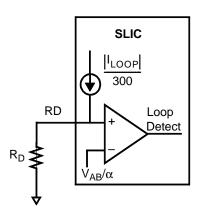


Figure 3. Loop Detect

For the Standby state, the A and B pins of the SLIC are each connected to the supplies through 200 Ω resistors. The B amplifier has a 7 V zener diode in series with the low battery. Much of the circuitry is shut down to save power. The following equation applies:

$$\frac{\left|V_{BATI}\right| - 10}{R_{LTH} + R_{SL} + 2R_F + 400} \, = \, \frac{915}{R_D}$$

OR

$$R_{\rm D} = \frac{(R_{\rm LTH} + R_{\rm SL} + 2R_{\rm F} + 400) \bullet 915}{|V_{\rm BATI}| - 10}$$

The Am79R79 RSLIC is designed such that the loop resistance, which causes a loop detect in the Standby state, is less than the loop-detect resistance in the Active state. This ensures that the loop still is detected as the SLIC moves from Standby to Active state. To guarantee this—even at the maximum battery voltage of –75 V—RD must be the minimum resistance of the values calculated in the preceding equations. A 75 k Ω value works in most applications, but RD must be at least 56 k Ω .

Some transients on DET can be expected as the SLIC changes state, and lasts approximately 10 ms. In most applications, you can write the microcontroller firmware to filter the transients.



AC CHARACTERISTICS

This section assumes the use of a simple codec, and that an op-amp is used for the transhybrid balance. (Some codecs, such as the SLACTM device, have the op-amp onboard. If you are using a SLAC device, you can set Z_T and Z_{RX} . You can choose a wide variety of real and complex two-wire impedances, transhybrid balances, and gains with the DSP filters in the SLAC device.)

In Figure 4, V_{IN} and V_{OUT} connect to the CODEC. Make the component calculations in this order: two-wire input impedance, receive path gain, transhybrid balance, and transmit path gain.

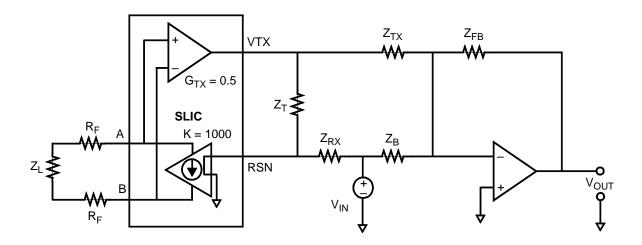


Figure 4. AC Model

Two-Wire Input Impedance

For maximum power transfer, terminate the loop in the complex conjugate of its characteristic impedance (specified by the regulatory agencies in each country). Z_T determines the input impedance (real or complex) of the SLIC. To calculate two-wire input impedance, Z_{2WIN} , replace Z_L with voltage source V_1 and let $V_{IN} = 0$.

Define:
$$Z_{2WIN} = \frac{V_1}{I_{LOOP}}$$

Write the loop equations:

(1)
$$V_{TX} = 0.5 \bullet (V_1 - I_{LOOP} \bullet 2R_F)$$

ALSO
$$I_{LOOP} = 1000 \bullet \frac{V_{TX}}{Z_{T}}$$

OR (2)
$$V_{TX} = \frac{Z_T \bullet I_{LOOP}}{1000}$$

Substitute (2) into (1)

$$\frac{Z_{T} \bullet I_{LOOP}}{1000} = 0.5 \bullet (V_{1} - I_{LOOP} \bullet 2R_{F})$$

$$\mbox{OR} \qquad Z_{\rm 2WIN} = \frac{V_1}{I_{\rm LOOP}} = \frac{Z_T}{500} + 2R_F \label{eq:ZWIN}$$

Now solve for Z_T:

$$Z_T = 500 \bullet (Z_{2WIN} - 2R_E)$$

To get a two-wire input impedance of 600 Ω with R_{F} = 50 $\Omega,$ then:

$$Z_{\rm T} = 2.5 \bullet 10^5 \Omega$$

Receive Path Gain

Gain from the four-wire side to the two-wire side, loaded, is G_{42L} . Be careful not to exceed the drive capability of the SLIC. Refer to the AC model in Figure 4 and write the loop equations.

Define:
$$G_{42L} = \frac{I_{LOOP} \bullet Z_L}{V_{IN}}$$

Write the loop equations:

(1)
$$I_{LOOP} = 1000 \bullet \left(\frac{V_{TX}}{Z_{T}} + \frac{V_{IN}}{Z_{RX}} \right)$$

(2)
$$V_{TX} = -0.5 \bullet I_{LOOP} \bullet (Z_L + 2R_F)$$

Substitute (2) into (1) and solve for I_{LOOP}/V_{IN} :

$$\frac{{\rm I_{LOOP}}}{{\rm V_{IN}}} = \frac{1000}{{\rm Z_{RX}}} \bullet \frac{1}{1 + \frac{500 \bullet ({\rm Z_L} + 2{\rm R_F})}{{\rm Z_T}}}$$

OR

$$G_{42L} = \frac{I_{LOOP} \bullet Z_L}{V_{IN}} = \frac{Z_T}{Z_{RX}} \bullet \frac{1000 \bullet Z_L}{Z_T + 500 \bullet (Z_L + 2R_F)}$$

Now solve for Z_{RX} :

$$Z_{RX} = \frac{Z_T}{G_{42L}} \bullet \frac{1000 \bullet Z_L}{Z_T + 500 \bullet (Z_L + 2R_F)}$$

Continuing the example above with $Z_T = 250 \text{ k}\Omega$, $Z_L = 600 \Omega$, $R_F = 50 \Omega$, and now $G_{42L} = \text{unity}$, then:

$$Z_{RX} = 2.5 \bullet 10^5 \Omega$$

Transhybrid Balance

A by-product of the two- to four-wire conversion is that some of the receive signal, V_{IN} , appears in the transmit path at the VTX pin. You must reduce this echo. Use the op-amp circuit to remove as much of this signal as possible from the transmitted signal.

To optimize transhybrid balance, use the following procedure. First, find the transfer function of V_{IN} to V_{TX} , called G_{44L} or four-wire return gain. Then calculate the impedance, Z_B , to cancel V_{TX} in the op-amp summing circuit. Notice that there is a 180° phase shift from V_{IN} to V_{TX} . If Z_L is resistive, Z_B also is resistive. If Z_L is complex, Z_B also is complex. Additionally, the SLIC contributes a small delay that you can adjust for by splitting Z_T and connecting a capacitor ($C_T = 60$ pF typical) from that junction to ground.

Determine G_{44L} (Refer to the AC Model in Figure 4) using the following equation:

Define:
$$G_{44L} = \frac{V_{TX}}{V_{IN}}$$

Write the loop equations:

(1)
$$V_{TX} = -0.5 \bullet I_{LOOP} \bullet (Z_L + 2R_F)$$

(2)
$$I_{LOOP} = 1000 \bullet \left(\frac{V_{TX}}{Z_{T}} + \frac{V_{IN}}{Z_{RX}} \right)$$



Substitute (2) into (1) and solve for V_{TX}/V_{IN}:

$$G_{44L} = \frac{V_{TX}}{V_{IN}} = \frac{-Z_{T}}{Z_{RX}} \bullet \frac{500 \bullet (Z_{L} + 2R_{F})}{Z_{T} + 500 \bullet (Z_{L} + 2R_{F})}$$

So that:

$$G_{441} = -0.583$$

Now calculate the component Z_{B} for the balance circuit. Again, write the loop equations around the circuit.

$$\frac{V_{TX} \bullet Z_{FB}}{Z_{TX}} + \frac{V_{IN} \bullet Z_{FB}}{Z_{B}} \; = \; 0 \label{eq:total_control_eq}$$

Z_{FB} drops out

$$\frac{V_{TX}}{Z_{TX}} = -\left(\frac{V_{IN}}{Z_{B}}\right)$$

OR

$$Z_B = -\left(\frac{Z_{TX}}{G_{44L}}\right)$$

If $Z_{TX} = 20 \text{ k}\Omega$, and $G_{44L} = -0.583$ as before, then

$$Z_{\rm B} = 34.31 \bullet 10^3 \ \Omega$$

and Z_{FB} sets the transmit path gain. The total load on V_{TX} must be greater than 20 k Ω to ensure proper operation of the RSLIC.

Transmit Path Gain

When adjusting the gain in the transmit path, do not exceed the input range of the codec. First, calculate the two- to four-wire gain, $G_{24}.$ The total transmit path gain is G_{24} multiplied by the gain through the op-amp. Refer to the AC Model in Figure 4 and substitute V_1 for $Z_L.$ Assume $V_{IN} = 0 \ V.$

Define:
$$G_{24} = \frac{V_{TX}}{V_1}$$

Write the loop equations:

(1)
$$V_{TX} = 0.5 \bullet (V_1 - I_{LOOP} \bullet 2R_F)$$

$$(2) \qquad I_{\text{LOOP}} = \frac{1000 \bullet V_{\text{TX}}}{Z_{\text{T}}}$$

Substitute (2) into (1) and solve for V_{TX}/V1:

$$G_{24} = \frac{V_{TX}}{V_1} = 0.5 \bullet \frac{Z_T}{Z_T + 2R_F \bullet 500}$$

So that: $G_{24} = 0.417$

For unity transmit path gain select:

$$\frac{Z_{FB}}{Z_{TX}} = \frac{1}{G_{24}}$$

If $Z_{TX} = 20 \text{ k}\Omega$, then:

$$Z_{FR} = 47.96 \bullet 10^3 \Omega$$

RINGING

The Am79R79 RSLIC generates a balanced ringing signal. During the Ringing state, V_A (TIP) and V_B (RING) alternate in polarity at a frequency determined by the RINGIN signal. In this way, you can obtain a peak-to-peak voltage of nearly twice the V_{BAT1} voltage, shown in Figure 5. Notice that the signal level relative to ground is always less in magnitude than V_{BAT1} . The ringing waveform is trapezoidal, with its slope controlled by the components R_{SLEW} and C_{SLEW} (see the *Crest Factor* section on page 7).

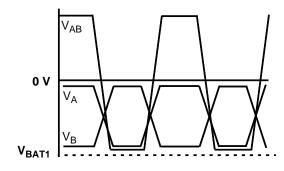


Figure 5. Balanced Ringing

Determine the ring-trip points, ring current limit, V_{BAT1} voltage and current ratings, and the crest factor. The current into the RSN node during the Ringing state sets the ringing current. The resistance used to set the current limit appears as the source resistance in the ring generator model. Therefore, loop length, V_{BAT1} voltage and current, and ring trip are all dependent on I_{RINGI IM}.

The order of calculation is: crest factor, $I_{RINGLIM}$, V_{BAT1} , and then ring trip.

Crest Factor

The crest factor (CF) of a waveform is the ratio of the peak (pk) value to its root-mean-square value. Thus, a waveform with a higher crest factor requires a higher peak value to get the same rms value. For example, a sine wave has a CF of 1.414, while a square wave has a CF of 1. TR909 requires a ringing voltage of 40 Vrms at the telephone set with a crest factor of 1.2 to 1.6. The Am79R79 RSLIC uses an external RC network connected to RINGIN to set CF. It is important that the voltage driving the network is centered at $V_{\rm CC}/2$, which is typically 2.5 V; otherwise, the ringing signal may appear to be a triangle wave on one or both polarities. Use a CMOS-level signal that has the same $V_{\rm CC}$ as the SLIC.

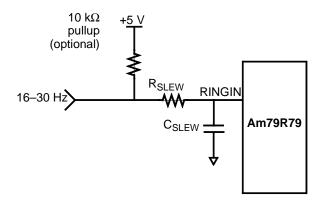


Figure 6. Crest Factor

Make sure that RINGIN toggles only while the SLIC is in Ringing state and that transitions in and out of ringing occur only when RINGIN is high. If RINGIN is low and the SLIC state changes from Ringing to Active, a fast voltage swing (not controlled by R_{SLEW} and C_{SLEW}) of approximately $V_{BAT1} + V_{APPH}$ results as the V_{AB} polarity reverses. The resulting capacitive discharge causes a short surge of current in the loop, which in turn causes a momentary \overline{DET} activation (up to 200 ms). Even if the state change is made with RINGIN high, there still can be as much as 100 ms of \overline{DET} activation, depending on capacitive loading of the line. You can write the firmware to filter out this condition.

$$CF = \frac{Per}{Per - (0.176 \bullet R_{SLEW} \bullet C_{SLEW})}$$

$$R_{SLEW} \bullet C_{SLEW} = \frac{(CF \bullet Per) - Per}{CF \bullet 0.176}$$

For example, assume you want a CF of 1.25 with a ringing frequency of 20 Hz. The product of R_{SLEW} and C_{SLEW} is 56.8 ms. To correctly bias the RINGIN input, use a value of 150 k Ω for R_{SLEW}, so C_{SLEW} is 0.39 μ F.

Ring Current Limit (IRINGLIM)

The ring current limit is set similarly to the DC current limit. The resistors R_{DCR1} and R_{DCR2} limit the current into the RSN node. The pin RDCR switches between +3 V and -3 V as the RINGIN signal switches. Choose capacitor C_{DCR} to provide a time constant of 15–150 μs . A current limit of approximately 11 mA per REN allows enough current to ring the phone and reliably ring trip.

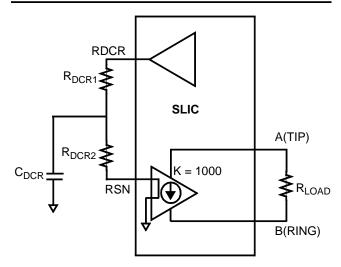


Figure 7. Ring Current Feed

Set I_{RINGLIM} at 11 mA per REN.

$$I_{RINGLIM} = \frac{3 \bullet 1000}{R_{DCR1} + R_{DCR2}}$$

$$\tau_{RING} = \frac{R_{DCR1} \bullet R_{DCR2}}{R_{DCR1} + R_{DCR2}} \bullet C_{DCR}$$

For light loads where R_{DCR1} + R_{DCR2} is greater than $80~k\Omega,~C_{DCR}$ can be eliminated.



VBAT1 Specification

 V_{BAT1} is set on the high end by the silicon process, but limit it to 75 V. Factors that determine the low end are loop length, crest factor, load (number of REN), fuse resistors, and the ring current limit resistors.

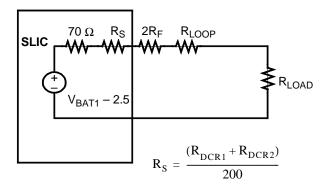


Figure 8. Simplified Ring Generator Model

TR909 requires a ringing voltage of 40 Vrms and a CF of 1.2–1.6. To determine V_{BAT1} , work backwards from the load using Ohm's Law. Using a value of 1.4 k Ω for a 5REN load, a current of 29 mArms is needed to get 40 Vrms. From the model, use the equation:

$$V_{BAT1} = I_{RING} \bullet CF$$

$$\bullet (R_{LOOP} + R_{LOAD} + 2R_F + R_S + 70) + 2.5$$

For example, if CF = 1.25, R_{LOAD} = 1.4 k Ω (5REN), R_{LOOP} = 100 Ω , I_{RINGLIM} = 55 mA, and R_F = 50 Ω ; then, R_S = 273 Ω and V_{BAT1} = 72.9 V.

If the load changes to 3REN, then I_{RING} must be 17.1 mArms, R_S = 455 Ω and V_{BAT1} = 68.0 V.

If you want to lower V_{BAT1} or drive a longer loop, leave $I_{RINGLIM}$ higher in order to lower R_S . For example, $R_S = 273~\Omega$ with 3REN results in $V_{BAT1} = 64~V$.

Ring Trip

A DC offset is traditionally required in the ringing signal for reliable ring-trip detection. This is due to the overlap of the AC impedance in the On-hook versus Off-hook states. In the central office, the DC impedance has a maximum value of 1.93 $k\Omega$ off hook and a minimum of 10 $k\Omega$ on hook. The AC impedance is a maximum 1.93 $k\Omega$ off hook and 1.23 $k\Omega$ minimum on hook, an overlap. Therefore, it's much easier to perform DC ring trip, since the impedance ratio is over 5.

With TR909, there is no overlap in either the DC or AC case. You do not need a DC offset, and AC detection is possible. The minimum on-hook impedance is 1.23 k Ω for AC and 10 k Ω for DC. The maximum offhook impedance for both is approximately 500 Ω .

For a 5REN load, an AC threshold of 900 Ω provides sufficient margin for reliable detection and you can raise it for lighter loads, if desired.

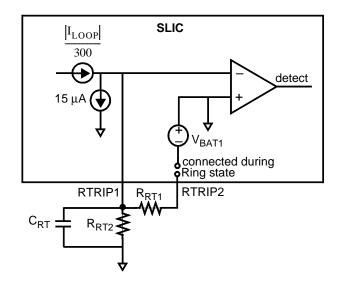


Figure 9. Ring-trip Detect

The ring-trip circuit is a current-threshold detector. A scaled version of the loop current is fed into $R_{RT1}.$ With no loop current, the voltage at RTRIP1 is negative. As loop current increases, so does $V_{RTRIP1}.$ When V_{RTRIP1} reaches 0, detect occurs. Because the loop current is changing polarity, there are nulls in the current, which in turn lower V_{RTRIP1} and cause detect to return to its inactive state.

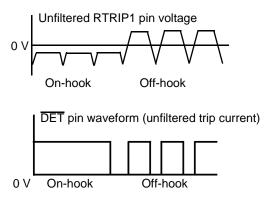


Figure 10. Ring-Trip Waveforms

 C_{RT} provides filtering that eliminates the \overline{DET} pin transition during the polarity switch. If $I_{RINGLIM}$ isn't high enough, some transients on \overline{DET} occur. R_{RT2} is a voltage divider, which keeps the RTRIP1 voltage between +3 V and -3 V.

Set I_{RINGLIM} high enough so that a change in current is detected when the phone goes off hook. That is why, even though only 6 mArms is needed to ring 1REN, 11 mA peak per REN is used as the current limit.

R_{RT1} is calculated from:

$$R_{\text{RT1}} = \frac{300 \bullet \text{CF} \bullet \text{V}_{\text{BAT1}} \bullet (R_{\text{LRT}} + R_{\text{S}} + 2R_{\text{F}})}{\text{V}_{\text{BAT1}} - 3.5 - \left[15 \bullet 10^{-6} \bullet 300 \bullet \text{CF} \bullet (R_{\text{LRT}} + R_{\text{S}} + 2R_{\text{F}})\right]}$$

Where R_{LRT} is the ringing level threshold resistance, set to $900~\Omega$ for 5REN or higher for lighter loads. (Refer to sections above for information on $R_S,$ CF, fuse resistors, and $V_{BAT1}.)$

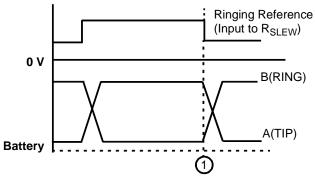
In the previous example, R $_{F}$ = 50 $\Omega,$ R $_{S}$ = 273 $\Omega,$ CF = 1.25, and V $_{BAT1}$ = 70 V. If R $_{LRT}$ is 900 $\Omega,$ then R $_{RT1}$ = 563 k $\Omega.$

The comparator input must remain between +3 V and -3 V. R_{RT1} and R_{RT2} form a voltage divider:

$$R_{RT2} < \frac{3 \bullet R_{RT1}}{V_{BAT1} - 3}$$

 C_{RT} has a time constant of 18 ms with R_{RT2} . A value of 22 k Ω for R_{RT2} results in a capacitor of 0.82 μ F.

You can minimize transients on DET by synchronizing the Am79R79 RSLIC state change with the ringing waveform, as shown in Figure 11.



Note:

1. The best time to switch between Ringing and other states to minimize detect switching transients.

Figure 11. Optimum Switching Time for Minimal Transients

APPLICATION SCHEMATIC

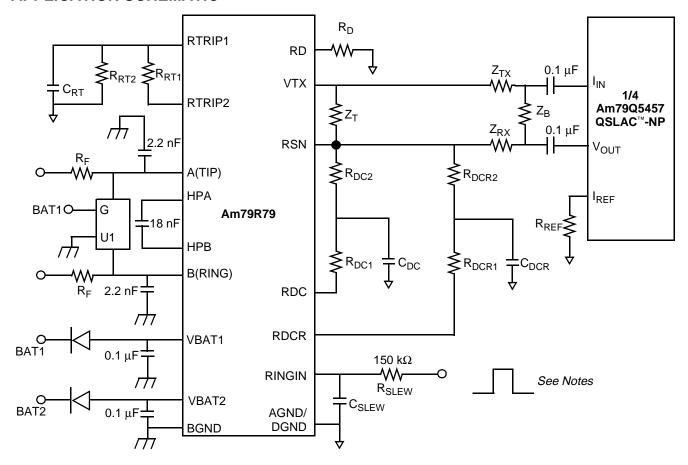


Figure 12. Application Circuit



Notes:

- The transmit path gain when using the QSLAC-NP differs slightly from the standard CODEC case. Replace Z_{FB} in the equation with 3R_{REF}.
- 2. The input to R_{SLEW} should be a 50% duty cycle, CMOS-compatible signal.
- 3. If the protection device U1 is needed, battery-reference it with the gate tied to BAT1.
- 4. R_{SGH} , R_{SGL} are left open in this example.
- 5. VNEG can be connected to BAT2 through a current limiting resistor.
- 6. The digital signals B2EN, DET, E1, D1, D2, and C3-C1 are not shown.
- 7. The 0.1 μF capacitors at the QSLAC-NP are for AC coupling and can be 20% tolerance of type X7R.
- 8. The 0.1 μ F capacitors on V_{BAT1} and V_{BAT2} are for supply de-coupling.
- 9. The 2.2 nF capacitors on A and B are for EMI susceptibility.
- 10. The 18 nF capacitor on HPA and HPB is a DC-blocking capacitor.
- 11. Not shown is the splitting of Z_T and the delay compensation capacitor, C_T .

ADDITIONAL REFERENCES

Am79R79 Ringing SLIC Data Sheet, PID# 19752B

Am79R79 Ringing SLIC Technical Overview, PID# 19768B

Am79R79 Ringing SLIC Device Call Processing Considerations Application Note, PID# 21781A

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